synertronixx GmbH, 2010-11-26

Embedded Socket Computer

SCB9328

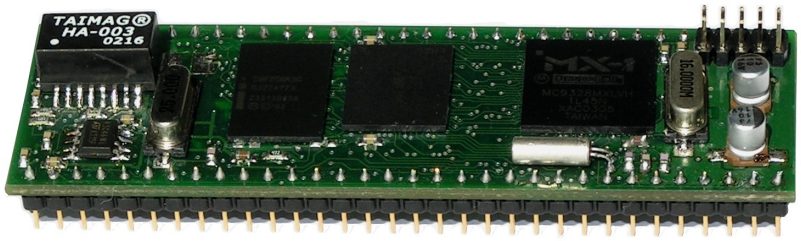

Figure 1: Embedded Socket Computer SCB9328

synertronixx GmbH
Vahrenwalder Straße 7
D-30165 Hannover
Tel.: 0511 / 93 57 670
Fax: 0511 / 93 57 679
Email: info@synertronixx.de
CEO: Dr. Matthias Blaschke, Marc-Oliver Borck
Ust-ID: DE 216 559 901
Steuer-Nr.: 25/208/13258
HRB: 59670, Amtsgericht Hannover
Stadtsparkasse Hannover
BLZ: 250 501 80
Kto: 27 80 84

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synertronixx GmbH
Vahrenwalder Straße 7
D-30165 Hannover
Tel.: 0511 / 93 57 670
Fax: 0511 / 93 57 679
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1 Introduction

The Embedded Socket Computer SCB9328 is a smart solution to expand your existing product line by including embedded ethernet and internet connections. The SCB9328 is based on a 200MHz Freescale™ MC9328MXL industrial-standard ARM9™ controller with 32 KBytes cache. It's standard JEDEC DIL-64 format modul makes it fast, extremely easy and affordable to add remote device management capabilities to electronic devices.

The CPU is based on the ARM™ RISC technology utilizing advanced 0.18µ process for high core speeds and performance (285K Dhrystone 2.1 per second). In a standard application with 100 MBit ethernet enabled the total power consumption is 0.7W typ. No fans or heatsinks are required which results in high reliability and zero noise. The Embedded Socket Computer SCB9328 is specially designed for high performance ethernet applications, requiring high network throughput rates on embedded computer modules. Typical applications include industrial automation systems, point-of-sale, data acquisition, building automation and control systems.

The SCB9328 is preinstalled with a bootloader, an embedded LINUX 2.6.20 or higher, a busy box and a preconfigured network interface. It is designed as a drop-in microcontroller replacement and contains the microprocessor core, the ethernet controller 16 MByte Flash and up to 32 MByte SDRAM. The modular approach in conjunction with a full featured LINUX offers significant advantages compared to full custom designs since it cuts down development times from month or years to days or weeks and shielding complex board technology from the user; e.g. fine pitch and

synertronixx GmbH Tel.: 0511 / 93 57 670 CEO: Dr. Matthias Blaschke, Marc-Oliver Borck Stadtsparkasse Hannover
Vahrenwalder Straße 7 Fax: 0511 / 93 57 679 Ust-ID: DE 216 559 901 BLZ: 250 501 80
D-30165 Hannover Email: info@synertronixx.de Steuer-Nr.: 25/208/13258 Kto: 27 80 84
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multilayer PCBs, BGA assembly and porting operating systems.

The following capabilities are supported by the SCB9328:

- **Network Protocols**
  ARP, IPV4, ICMP, UDP, TCP, HTTP, DHCP, TFTP, FTP, POP3, SMTP, SCP
- **Network Interface**
  10/100MBit IEEE 802.3 Ethernet interface
  On-board magnetics
  Pre-programmed MAC-address
- **Device Interface**
  Serial port (up to 1MBaud)
  I²C interface
  USB device support
  Data- and Addressbus

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2 SCB9328 Features

- Single power supply (3.3 V / 400 mA. max.)
- Flash memory on-board (8, 16, 32 MByte)
- 32-bit SDRAM (16, 32 MBytes)
- Freescale™ i.MXL 200MHz ARM9™ CPU
- Virtual memory management unit (VMMU)
- Davicom DM9000 10/100 Mbit/s fast ethernet controller
- Full speed (12 MHz) USB 1.1 device support
- High speed UART (up to 1 Mbit/s)
- I^2C-Interface (up to 2,4 MHz clock)
- 13 Low Voltage CMOS GPIOs
- Integrated realtime clock
- On-board reset controller
- Programmable watchdog timer
- External 16-bit databus, 18-bit addressbus interface
- JEDEC standard 64-pin DIL package (84 x 27mm)
- JTAG test interface

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3 Embedded Software

- Embedded Linux 2.6.20 or higher
- Bootloader uboot 1.2.0
- Board support package for Freescale™ i.MXL CPU
- DM 9000 ethernet packet driver
- Driver support for UART, I^2C and GPIO
- Journaling flash file driver JFFS2
- TCP/IP stack
- Integrated HTTP and FTP-server

4 i.MXL Processor

The MC9328MXL CPU is an ARM920T™ 32-bit RISC core running at 200 MHz, while system speed is running at 72 MHz. The ARM920T™ is based on the ARM9TDMI™ Harvard architecture processor core, with an efficient 5-stage pipeline. Its internal bus architecture and fast system speed provides an outstandig performance which is an ideal solution for network and wireless applications.

The ARM920T™ processor core consists of a 32-bit data path and associated control logic. This data path contains 31 general purpose registers, coupled to a full shifter, Arithmetic Logic Unit and multiplier. At any one time 16 registers are visible to the user. The remainder are synonyms used to speed up exception processing. Register 15 is the Program Counter (PC) and can be used in all instructions to reference data relative to the current instruction. R14 holds the return address after a

synertronixx GmbH Tel.: 0511 / 93 57 670 CEO: Dr. Matthias Blaschke, Marc-Oliver Borck Stadtsparkasse Hannover
Vahrenwalder Straße 7 Fax: 0511 / 93 57 679 Ust-ID: DE 216 559 901 BLZ: 250 501 80
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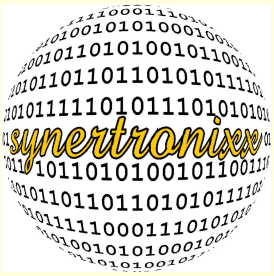

subroutine call. R13 is used (by software convention) as a stack pointer.

Two 16 kByte caches are implemented, one for instructions, the other for data, both with an 8-word line size. A 32-bit data bus connects each cache to the ARM9TDMI™ core allowing a 32-bit instruction to be fetched and fed into the instruction decode stage of the pipeline at the same time as a 32-bit data access for the Memory stage of the pipeline.

Cache lock-down is provided to allow critical code sequences to be locked into the cache to ensure predictability for real-time code. The cache replacement algorithm can be selected by the operating system as either pseudo random or round-robin. Both caches are 64-way set associative. Lock-down operates on a per-set basis. The ARM920T™ processor also incorporates a 16-entry write buffer, to avoid stalling the processor when writes to external memory are performed.

The main important features of the MC9328MXL are:

- 200 MHz processing speed
- 16K instruction cache and 16K data cache
- ARM9™ high performance 32-bit RISC engine
- Thumb® 16-bit compressed instruction set for a leading level of code density
- EmbeddedICE™ JTAG software debug
- 100-percent user code binary compatibility with ARM7TDMI® and StrongARM processors
- Cache locking to support mixed loads of real-time and user applications

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5 Memory

The SCB9328 is assembled with up to 32 MByte of 32-bit SDRAM and 16 MByte of fast access NOR Flash. The memory interface is designed for fast start-up times and high throughput rates. The system speed of the both memories is 72 MHz. Customer variations of the memory size can be assembled on request.

The ARM9™ core uses a flat memory model. All internal as well as the external peripherals are mapped into the 4 GBytes address spaces of the MC9328MXL CPU.

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6 Bock Diagramm

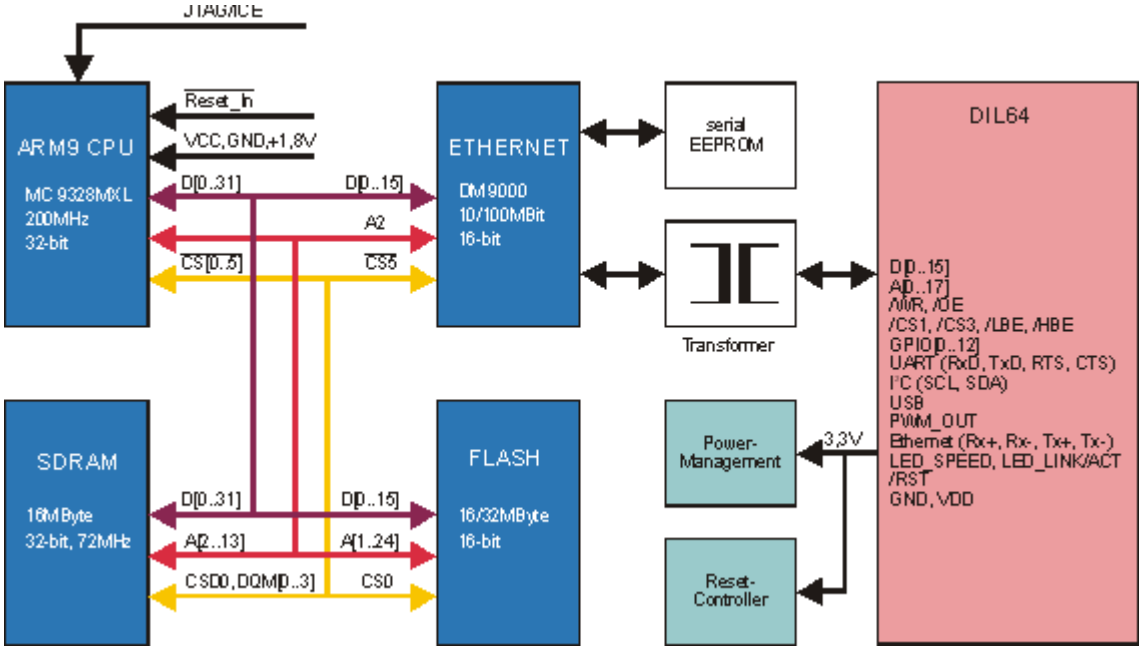

Figure 2: Block Diagramm

7 GPIOs

External peripherals like low-current LEDs and switches can connected directly to the SCB9328. Any GPIO pin is LV-CMOS compatible. The GPIO pins are multiplexed with the UART, I2C and USB-Pins. After power-up the GPIO pins are configured as inputs and the alternative functions are disabled. All GPIOs have internal 70k pull-up resistors. The GPIO-pins are not 5V tolerant.

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8 Ethernet Interface

The SCB9328 provides a 10BASE-T/100BASE-TX Davicom DM9000 10/100 Mbit Fast Ethernet MAC/PHY which is fully compatible with the IEEE802.3 standard. On chip features are a 8 kByte internal transmit and receive FIFO and a quasi DMA interface to the processor bus (sequential write/read access). Half-duplex and full-duplex modes are supported for both 10 Mbit and 100 Mbit operations with embedded RAM for packet buffering. The Davicom DM9000 is connected to the MC9328MXL in 16-bit mode.

The SCB9328 is especially designed for high performance network applications. Data rates up to 60Mbit/s are achievable.

9 UART

The UART provides serial communication capability with external devices through an RS-232 interface. UART transmit and receive characters can either 7 or 8 bits in length (program selectable). The UART also contains a configurable auto baud detection circuitry to receive 1 or 2 stop bits as well as odd, even, or no parity. The UART generate baud rates based on a configurable divisor and input clock. The receiver detects framing errors, idle conditions, BREAK characters, parity errors and overrun errors.

An additional feature is the 32 Byte deep receive and transmit FIFO which effectively reduce software overhead. The signals TxD, RxD, CTS and RTS are accessible on the DIL-64 socket. The UART pins are not 5V tolerant.

synertronixx GmbH Tel.: 0511 / 93 57 670 CEO: Dr. Matthias Blaschke, Marc-Oliver Borck Stadtsparkasse Hannover
Vahrenwalder Straße 7 Fax: 0511 / 93 57 679 Ust-ID: DE 216 559 901 BLZ: 250 501 80
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10 I²C

I²C is a two-wire bidirectional serial bus that provides a simple and efficient method of data exchange while minimizing the interconnection between devices. The flexible I²C bus allows additional devices to be connected to the bus for expansion and system development. The I²C can be configured as master or slave. Multi-master configurations are supported by featuring collision and arbitration detection to prevent data corruption.

The I²C interface uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. For I²C compliance, all devices connected to these two signals must have open drain or open collector outputs with an additional pull-up resistor. The I²C interface supports 3.3V tolerant devices. 64 different frequencies are supported by software programmable clock generation. The max. programmable clock rate is 2.4 MHz. The SCL and SDA pins are not 5V tolerant.

11 USB

The SCB9328 provides USB device support with full speed operation (12 MHz). The USB interface is USB 1.1 compatible. Bulk, Interrupt and Isochronous pipes are supported. An external USB PHY is necessary to connect the SCB9328 to an USB-network. The USB interface pins are not 5V tolerant.

synertronixx GmbH Tel.: 0511 / 93 57 670 CEO: Dr. Matthias Blaschke, Marc-Oliver Borck Stadtsparkasse Hannover
Vahrenwalder Straße 7 Fax: 0511 / 93 57 679 Ust-ID: DE 216 559 901 BLZ: 250 501 80
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12 Timers

Two independent timers are provided in the MC9328MXL CPU. They can be programmed to generate interrupts after expiration of times. An individual PLL timer clock provides non-fractional ratios between system speed and the internal timer clock which makes the external peripheral bus independand from the core speed

13 Watchdog

An 8/16-bit data bus and a 18-bit address bus are provided for connecting external peripherals to the SCB9328. Any external bus pin is LV-CMOS compatible. Two individually programmable chip selects (/CE1, /CE3) and a /OE and /WR signal allow using a wide range of 8- and 16-bit peripherals to be connected directly to the SCB9328. Each chip select has programmable access time settings which allows mixing fast and slow peripherals on the same databus. By using the /LBE and /HBE signals external memory can accessed byte wide.

It is highly recommended to use external busdrivers when connecting external hardware to the SCB9328 because capacitive bus loads have an significant influence to the bus timing of the i.MXL processor. The external peripheral bus is not 5V tolerant.

14 External Peripheral Bus

synertronixx GmbH Tel.: 0511 / 93 57 670 CEO: Dr. Matthias Blaschke, Marc-Oliver Borck Stadtsparkasse Hannover
Vahrenwalder Straße 7 Fax: 0511 / 93 57 679 Ust-ID: DE 216 559 901 BLZ: 250 501 80
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15 Interrupts

Each input port of the SCB9328 can be programmed individually as an interrupt source. The interrupt source can be routed as standard or as fast interrupt source. Any external interrupt can be programmed as level sensitive or as rising or falling edge sensitive interrupt.

16 Reset

A power-on reset generator with low voltage detection resets all components on the the module. An external reset signal (not 5V tolerant) can be used to reset the processor core. A low voltage detection prevents the module of corrupting data of the Flash device.

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17 Bootloader

The SCB 9328 is shipped with a preinstalled bootloader uboot 1.2.0. The bootloader can be disabled in order to start immediately the operating system. Only a simple PC terminal program is necessary to work with the bootloader. Downloads can performed over the serial interface or ethernet. The uboot bootloader uses a TFTP server for downloading programs. The download option over ethernet results in highly reduced download and update times.

18 Linux

The SCB9328 contains a preinstalled, full featured and performance optimised LINUX (kernel version 2.6.20 or higher) operating system with TCP/IP, embedded Web server, FTP server, Telnet server and Journaling flash file system support. The embedded LINUX contains all necessary drivers for controlling the UART, ethernet, I^2C and the GPIO ports.

For a seamless SCB9328 Windows integration an optional SAMBA suite provides directory and file services as well as account controls to Windows clients. By using SAMBA the SCB9328 can directly integrated into Windows networks providing easiest data exchange with Windows PCs. No additional software is required when using the SCB9328 with SAMBA in existing Windows networks.

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19 Flash Memory Partitions

The flash memory of SCB9328 is divided into 5 partitions. The following table 1 show the usage of the flash file system:

Table 1: Flash Memory Partitions

Physical Address	Description	Size
0x0000 0000 **0x0001 FFFF**	Bootloader uboot	128 kByte
0x0002 0000 **0x0003 FFFF**	uboot Environment	128 kBytes
0x0004 0000 - **0x0023 FFFF**	LINUX 2.6.20 kernel or higher	2 MByte
0x0024 0000 - **0x00FF FFFF**	Root File System	14.75 MBytes

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20 Memory Map

Table 2: Memory Map

Physical Address	Description	Chip-Select MC9328MXL	Size
0x0000 0000 - 0x000F FFFF	Double MAP Image	/CS0	1 MBytes
0x0010 0000 - 0x001F FFFF	Bootstrap ROM	internal	1 MBytes
0x0020 0000 - 0x0022 6FFF	Internal Registers	internal	156 KBytes
0x0022 7000 - 0x002F FFFF	Reserved	n.a.	868 KBytes
0x0030 0000 - 0x07FF FFFF	Reserved	n.a.	125 MBytes
0x0800 0000 - 0x0BFF FFFF	SDRAM	/CSD0	64 MBytes
0x0C00 0000 - 0x0FFF FFFF	Reserved for future use	/CSD1	64 MBytes
0x1000 0000 - 0x11FF FFF	Flash	/CS0	32 MBytes
0x1200 0000 - 0x12FF FFFF	External /CS1	/CS1	16 MBytes
0x1300 0000 - 0x13FF FFFF	Reserved for future use	/CS2	16 MBytes
0x1400 0000 - 0x14FF FFFF	External /CS3	/CS3	16 MBytes
0x1500 0000 - 0x15FF FFFF	Reserved for future use	/CS4	16 MBytes
0x1600 0000 - 0x16FF FFFF	Ethernet	/CS5	16 MBytes
0x1700 0000 - 0x4FFF FFFF	Reserved	n.a.	912 MBytes
0x5000 0000 - 0x5000 0FFF	ARM Test Registers	n.a.	4 KBytes
0x5000 1000 - 0xFFFF FFFF	Reserved	n.a.	2816 MBytes

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21 Pin Descriptions

Table 3: Description of Pin Numbers and its function

Pin Group	Pin Name	Pin Number	Direction	Function
CPU Bus	D0-D7 D8-D15	31-24 33-40	I/O	Bidirectional Data bus
	A0-A17	23-6	Out	Address bus
	/OE	2	Out	Read Enabe. Pin is directly connected to the /OE-Pin of the MC9328MXL. Read enable is low active.
	/WR	3	Out	Write Enable. Pin is directly connected to the R/W-Pin of the MC9328MXL. Write Enable is low active.
	/CS1 /CS3	5 4	Out Out	Chip Select. Pins are directly connected to the /CS1 and /CS3-Pins of the MC9328MXL
	/LBE /HBE	44 43	Out	Byte enable. /LBE is the strobe signal for D[0..7], /HBE is the strobe signal for D[8..15]. Pins are directly connected to the /EB3 and /EB2-Pins of the MC9328MXL
Power	/RES	42	In	Master reset input. Internal 70k Pullup.
	GND	32	Power	Ground
	VDD	64	Power	Positive Power Supply

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Table 4: Pin configuration of the USB interface

Pin Group	Pin Name	Pin Number	Direction	Function
USB Interface	VMO, VPO	51, 50	Out	USB Module Data Output. These signals provide single ended data to the USB Transceiver Transmitter differential driver.
	VM, VO	49, 48	In	Input D+/D- signal connected directly to the D+ and D- of the MC9328MXL respectively
	SUSPND	47	Out	Transceiver Suspend Enable. This signal, when high, activates a low-power state in the USB transceiver. Normally, when suspended, the transceiver drives USBD_RCV low and tri-state the USB bus signals D+ and D-.
	RCV	46	In	USB Module Receive Data. This signal is a CMOS level driven signal provided by the external USB transceiver. The signal is derived from the D+ and D- differential input to the transceiver.
	ROE	45	Out	Reverse Output Enable. This active low signal is used to control the transceiver to drive its D+/D- signal (to the host connection) according to the signal in USBD_VPO and USBD_VMO (output signal), respectively.

synertronixx GmbH Tel.: 0511 / 93 57 670 CEO: Dr. Matthias Blaschke, Marc-Oliver Borck Stadtsparkasse Hannover
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Table 5: Pin configuration of the Ethernet-, Timer- and PWM interface

Pin Group	Pin Name	Pin Number	Direction	Function
Ethernet	LED_LINK	58	Out	LED activity. This pin acts as LED_RX as well as link indicator. LED_LINK is low active.
	LED_SPEED	59	Out	LED speed. This pin acts as speed indicator. It is active when the 100 Mbit signal is detected. LED_SPEED is low active.
	ETH_TX+, ETH_TX-	63, 62	Out	This pair carries the 10/100 Mbit differential transmit output. The output Manchester encoded signals have been pre-distorted to prevent overcharge on the twisted-pair media and thus reduce jitter. ETH_TX+ and ETH_TX- are fed through internal magnetics. No external magnetics required.
	ETH_RX+, ETH_RX-	61, 60	In	This input pair receives the 10/100 Mbit differential Manchester encoded data from the twisted-pair wire. ETH_RX+ and ETH_RX- are fed through internal magnetics. No extenal magnetics required.
Timer Interface	TIN	1	In	Counter Input to Timer. This signal is directly connected to the MC9328MXL
PWM Interface	PWM_OUT	41	Out	PWM out. This signal is directly connected to the MC9328MXL

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Table 6: Pin configuration GPIO Port, the UART and the I²C interface

Pin Group	Pin Name	Pin Number	Direction	Function
GPIO Port	GPIO[0..12]	45-57	I/O	General purpose I/O Port. Pins are directly conntected the port pins of the MC9328MXL. GPIO[0..6] is connected to PB[21..27]. GPIO [7..8] is connected to PA[14..15]. GPIO[9..12] is connected to PC[9..12]. The GPIO-Port is shared with the I²C-Interface, the USB-Interface and the UART.
UART	RxD TxD CTS RTS	57 56 55 54	In Out In Out	Serial Interface. RxD and TxD Pins are directly connectet to the UART1 RxD and TxD pins of the MC9328MXL. CTS is connected to PC10, RTS is connected to PC9 of the MC9328MXL in order to maintain DTE convention (cross connection).
I²C Interface	SCL SDA	53 52	Out I/O	Bidirectional I²C-Interface.

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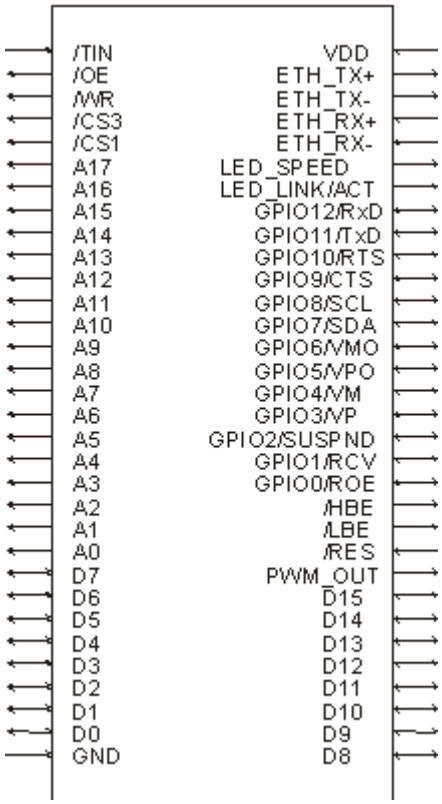

Figure 3: Pin Configuration

synertronixx GmbH
Vahrenwalder Straße 7
D-30165 Hannover
Tel.: 0511 / 93 57 670
Fax: 0511 / 93 57 679
Email: info@synertronixx.de
CEO: Dr. Matthias Blaschke, Marc-Oliver Borck
Ust-ID: DE 216 559 901
Steuer-Nr.: 25/208/13258
HRB: 59670, Amtsgericht Hannover
Stadtsparkasse Hannover
BLZ: 250 501 80
Kto: 27 80 84

22 JTAG Header Pinout

Table 7: Pin configuration of the JTAG interface

Pin Group	Pin Name	Pin Number	Direction	Function
JTAG RM2mm Header	/TRST	1	OUT	Test Reset Pin
	TCK	3	OUT	Test Clock
	/TDO	5	OUT	Serial Output
	TDI	7	I/O	Serial Input
	TMS	9	I/O	Test Mode Select
	/RES	2	IN	Reset Input
	GND	4, 6, 8, 10	SUPPLY	Ground

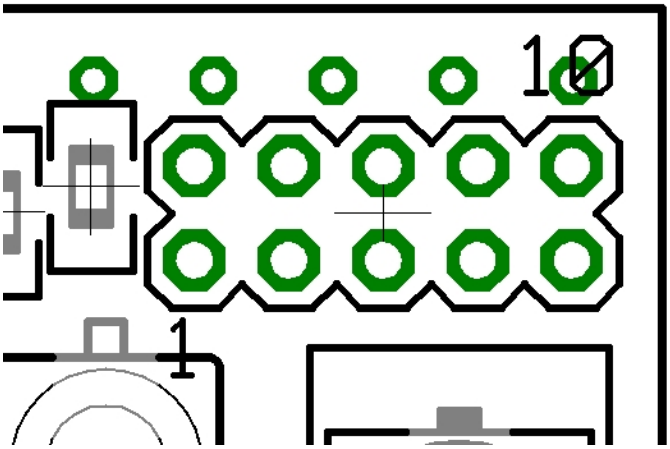

Figure 4: JTAG interface

synertronixx GmbH
Vahrenwalder Straße 7
D-30165 Hannover
Tel.: 0511 / 93 57 670
Fax: 0511 / 93 57 679
Email: info@synertronixx.de
CEO: Dr. Matthias Blaschke, Marc-Oliver Borck
Ust-ID: DE 216 559 901
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23 Electrical Characteristics

Table 8: Absolute Maximum Ratings

Rating	Symbol	Minimum	Maximum	Unit
Supply voltage	V_{DD}	-0.3	3.3	V
Output high current	$I_{OH,MAX}$		4.0	mA
Output low current	$I_{OL,MAX}$	-4.0		mA
Flash Block Write Cycles		100k		cycles
Maximum operating temperature range	T_A	0	70	°C
Storage temperature		-10	85	°C

Table 9: Recommended Operating Range

Rating	Symbol	Minimum	Maximum	Unit
Supply voltage	V_{DD}	3.135	3.3	V
I/O voltage	V_{IO}	-0.3	3.3	V

synertronixx GmbH
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D-30165 Hannover
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Fax: 0511 / 93 57 679
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DC Electrical Characteristics

Table 10: Electrical Characteristics (DC), T_A=25°C

Number or Symbol	Parameter	Minimum	Typical	Maximum	Unit
I_{DD}	Full operating current with ethernet enabled		210	400	mA
V_{IH}	Input high voltage	0.7 V_{DD}		V_{DD}+0.2	V
V_{IL}	Input low voltage			0.4	V
V_{OH}	Output high voltage (I_{OH} = 2.0mA)	0.7V_{DD}		V_{DD}	V
V_{OL}	Output low voltage (I_{OL} = -2.5mA)			0.4	V
V_{PTP}	Power-on voltage trip point	2.85	2.93	3.0	V
t_{PRT}	Power-on reset time		350		ms

synertronixx GmbH Tel.: 0511 / 93 57 670 CEO: Dr. Matthias Blaschke, Marc-Oliver Borck Stadtsparkasse Hannover
Vahrenwalder Straße 7 Fax: 0511 / 93 57 679 Ust-ID: DE 216 559 901 BLZ: 250 501 80
D-30165 Hannover Email: info@synertronixx.de Steuer-Nr.: 25/208/13258 Kto: 27 80 84
HRB: 59670, Amtsgericht Hannover

24 Mechanical Dimensions

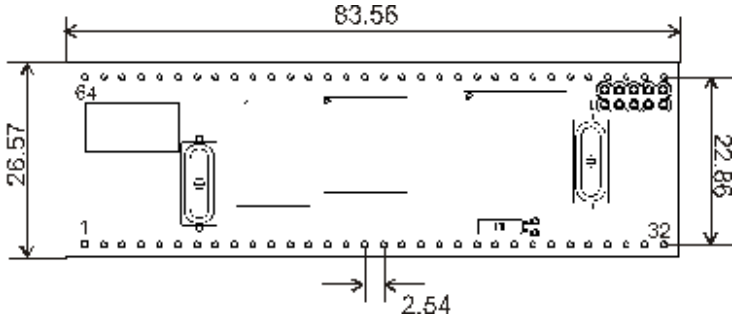

Figure 5: Mechanical Dimensions

25 Ordering Information

Ordering information for the SCB 9328 socket computer boards. (Please have a look at table 11)

Table 11: Available socket computer boards

Ordering Number	Clock	SDRAM	Flash
SCB9328-200/16/8*	200 MHz	16 MByte	8 MByte
SCB9328-200/16/16	200 MHz	16 MByte	16 MByte
SCB9328-200/32/16**	200 MHz	32 MByte	16 MByte
SCB9328-200/32/32**	200 MHz	32 MByte	32 MByte

* The SCB9328-200/16/8 is available on request. Minimum quantity is 500 pcs.
** The SCB9328-200/32/16 and SCB9328-200/32/32 are available on request. Minimum quantity is 100 pcs.

synertronixx GmbH Tel.: 0511 / 93 57 670 CEO: Dr. Matthias Blaschke, Marc-Oliver Borck Stadtsparkasse Hannover
Vahrenwalder Straße 7 Fax: 0511 / 93 57 679 Ust-ID: DE 216 559 901 BLZ: 250 501 80
D-30165 Hannover Email: info@synertronixx.de Steuer-Nr.: 25/208/13258 Kto: 27 80 84
HRB: 59670, Amtsgericht Hannover

26 Life Support Applications

SCB9328 Embedded Socket Computer are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. synertronixx customers who using or selling these products for use in such applications do so at their own risk and agree to fully indemnify synertronixx for any damages resulting from such improper use or sale.

27 Contacts

synertronixx GmbH
Vahrenwalder Str. 7
D-30165 Hannover

Email: info@synertronixx.de
Internet: www.synertronixx.de